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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/079,472
Filing Date: February 19, 2002
Appellant(s): MAHAJANI ET AL.

Pamela J. Squyres
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 28 Nov. 2005 appealing from the Office action mailed 20 Apr. 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,674,138	Halliyal et al.	01-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 9, 12-15, 24, 26, 36-37 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6674138 to Halliyal et al.

Regarding to claims 9, 24 Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, column 9 line 1, and providing a first oxide layer 28 on the channel region by ISSG process, column 10 line 33, providing a silicon nitride layer 30, column 1 line 41, on the first oxide layer 28, and providing a second oxide layer 32, column 8 line 63, on the silicon nitride layer 30, wherein the device is a SONOS.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20.The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41.

Thus Halliyal either inherently or implicitly discloses nitride layer

Regarding claims 12-15, Halliyal discloses a method wherein the ISSG is performed at a temperature ranging from 700°C to about 1150°C, column 11 line 17, wherein the pressure ranging from 100 torr to about 300 torr, column 11 line 9, wherein the ISSG oxide layer 28 having the thickness of 10 to about 150 angstrom, column 11 line 65, wherein the transistor is a SONOS transistor, wherein the method further including annealing the oxide layer 18 in a nitric oxide atmosphere, column 7 line 39.

Regarding claim 26, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by the method comprising: providing polysilicon 16, column 10 line 3, providing a first oxide layer 28 on the silicon layer 16 by ISSG, column 10 line 33, providing a silicon nitride layer30, column 1 line 41, on first oxide layer, and providing a second oxide layer 32, column 8 line 63, on the silicon nitride layer 30, wherein the device is a SONOS device.

With respect to silicon nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41.

Thus Halliyal either inherently or implicitly discloses nitride layer

Regarding claims 36, 37, Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, providing a first oxide layer 28 in contact with the channel region by an in-situ steam generation process, column 10 line 33, providing a silicon nitride layer 30, column 1 line 41, in contact with the first oxide layer 28; and providing a second oxide layer 32, column 8 line 63 in contact with the silicon nitride layer 30, fig. 1.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the

nitride layer 30 of the conventional ONO, column 12 lines 15-20. The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41. Thus Halliyal either inherently or implicitly discloses nitride layer

Regarding claim 38, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by a method comprising: providing a silicon wafer or silicon layer 16, fig. 1, providing a first oxide layer 28 in contact with the silicon wafer or silicon layer 16 by an in-situ steam generation process, column 10 line 33, providing a silicon nitride layer 30, column 1 line 41, in contact with the first oxide layer; and providing a second oxide layer 32 in contact with the silicon nitride layers, fig. 1, wherein the device is a SONOS semiconductor device.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41. Thus Halliyal either inherently or implicitly discloses nitride layer.

(10) Response to Argument

Appellant's arguments filed 28 Nov. 2005 have been fully considered but they are not persuasive.

a. Issue A: claims 9, 12-15, and 24 are not anticipated by Halliyal. The Appellant argues in page 11 lines 9-10 that each layer is formed on the one before it, so this is a contiguous stack, with no other layers intervening in page 11 lines 9-10, and layer 30 of Halliyal cannot be characterized as a silicon nitride layer in page 11 line 15. The examiner respectfully disagrees because the contiguous stack is not recited in the rejected claimed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is the claims, not specification that are anticipated or unpatentable. In Constant v. Advanced Micro Device Inc. 7 USPQ2d 1064. Therefore, Applicant cannot read limitation only set forth in the description into the claim for the purpose of avoiding the prior art. In re. Sporck, 386 F. 2d 924,155 USPQ 687 (CCPA 1967).

With respect to 'layer 30 cannot be characterized as a silicon nitride layer', the Examiner respectfully disagrees because Halliyal discloses layer 30 comprises ONO (silicon oxide = O, silicon nitride = N), col. 1 lines 33 and 41. The layer 30 is being modified by using a composite material, col. 12 line 9, including high-K and standard-K dielectric materials, col. 12 lines 11-20, or high-K dielectric material layer is sandwiched between two nitride layers, col. 12 lines 23-30. The standard-K dielectric material is silicon

nitride, col. 5 lines 42-47. By reading the disclosure of Halliyal, one of ordinary skill in the art would understand that layer 30 comprises silicon nitride layer deposited on the first oxide layer 28. The claim does not exclude the composite silicon nitride. Thus, the Examiner submits that layer 30 of Halliyal can be characterized as silicon nitride layer and meets the claim limitation. It has been held that the use of the term "comprising" leaves a claim open for inclusion of material or steps other than recited in the claims. Ex parte Davis, 80 USPQ 448 (PTO Bd. App. 1948). Use of the term « comprising » does not exclude the presence of the element. In re Hunter, 288 F. 2d 930, 129 USPQ 25 (CCPA 1961).

b. Issue B: Claims 26 and 36-38 are not anticipated by Halliyal et al. The Appellant argue that the substrate 16 is formed in a monocrystalline silicon substrate in page 14 line 5. The Examiner respectfully disagrees because it appears that the Appellant has misinterpreted the substrate 16 of Halliyal. First, Halliyal discloses the substrate 16 or 44 in fig. 6 comprises P-doped silicon, SOI, SOS, bulk silicon, and semiconductor substrates formed of other material know in the art, col. 9 line 45-50, and polysilicon, col. 9 line 60. In addition to monocrystalline silicon as a substrate, Halliyal clearly discloses the substrate can be including polysilicon, col. 9 line 60. Second, silicon (semiconductor) has three known crystal structures: polycrystal, monocrystal, and amorphous that has been

well documented by Mitsuhiro (US Pat. 6281427) in col. 2 lines 39-41, Watanabe (US Pt. 5316960) in 4 lines 22-26, Kubota (US Pat. 5754155) in col. 10 lines 37-40, and Kusumoto (US Pat. 6348369) in col. 1 lines 14-17. Third, the interpretation of the word 'polysilicon' would simply mean that 'many or more than one silicon elements or atoms'. Such 'polysilicon' layer or substrate may have different crystal orientation structure and the claim language has failed to identify the crystal structure of the substrate. Thus, the examiner submits that the silicon substrate 16 of Halliyal would comprise multiple silicon atoms or elements bonding together forming a 'polysilicon substrate' and would read on the claim limitation.

With respect to 'SONOS' and 'polysilicon channel region', Halliyal clearly discloses a SONOS structure (16 = silicon or S, 28 = oxide or O, 30 = composite nitride or N, 32 = oxide or O, and 24 = silicon or S, col. 1 lines 35 and 40. As discussed in the above, the substrate 16 of is a 'polysilicon substrate' and the channel 18 (a region between source and drain), col. 5 line 8, is a polysilicon channel and oxide layer 28 is in contact with the channel region 18, the nitride layer 30 is contact with the oxide layer 28, and second oxide layer 32 is in contact with nitride layer 30, fig. 1. Thus, Halliyal would read on the claim limitations.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Thao X. Le TL
06 Feb. 2006

Conferees:

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